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- ☐ 2. **Constraint driven pin mapping for concurrent SOC testing**
Yu Huang; Nilanjan Mukherjee; Chien-Chung Tsai; Samman, O.; Yahya Zaidan; Yanping Zhang; Wu-Tung Cheng; Reddy, S.M.;
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- ☐ 3. **Static pin mapping and SOC test scheduling for cores with multiple test sets**
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- ☐ 4. **Standard automatic test system (SATS) hardware interface standards for SATS frameworks, VXI instrument front panels, power module interface, augmentation module interface, receiver fixture interface, pin map configuration**
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- ☐ 5. **"ATE open system platform" IEEE-P1552 structured architecture for test systems (SATS)**
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